Amendments to the Claims

This listing of claims will replace all prior versions and listings of claims in the application.

Listing of Claims:

Claims 1 - 8 (canceled)

Claim 9-10 (cancelled)

Claim 11 (withdrawn): A solder configuration, comprising a pad having a surface upon which an intermetallic boundary interface is disposed, said intermetallic boundary interface defining a separation between said pad and solder that forms part of a solder joint, said intermetallic boundary interface being characterized as non-planar and having a plurality of steps, whereby a crack forming in said solder is influenced to proceed along said interface with a non-planar, stepped path, thereby lengthening its travel, and preventing failure of said solder joint.

Claim 12 (withdrawn): A solder configuration, comprising a pad having a surface upon which an intermetallic boundary interface is disposed, said intermetallic boundary interface defining a separation between said pad and solder that forms part of a solder joint, said intermetallic boundary interface being characterized as non-planar and having a plurality of concentric interruptions, whereby a crack forming in said solder is influenced to proceed along

said interface with a non-planar, interrupted path, thereby lengthening its travel, and preventing failure of said solder joint.

Claim 13 (withdrawn): A solder configuration, comprising a pad having a surface upon which an intermetallic boundary interface is disposed, said intermetallic boundary interface defining a separation between said pad and solder that forms part of a solder joint, said intermetallic boundary interface interface being characterized as non-planar and having a plurality of interdigitated interruptions, whereby a crack forming in said solder is influenced to proceed along said interface with a non-planar, interrupted path, thereby lengthening its travel, and preventing failure of said solder joint.

Claim 14 (withdrawn): A solder configuration, comprising a pad having a surface on which an intermetallic boundary interface is disposed, said intermetallic boundary interface defining a separation between said pad and solder that forms part of a solder joint, said intermetallic boundary interface being characterized as non-planar and having a cross-shaped interruption, whereby a crack forming in said solder is influenced to proceed along said interface with a non-planar, interrupted path thereby lengthening its travel, and preventing failure of said solder joint.

Claim 15-16 (cancelled)

Claim 17 (currently amended) A solder joint for interconnecting an electronic chip to a substrate, comprising:

a metallic pad having a substantially planar lower surface for engaging said substrate and an upper surface extending in a first plane;

an obstacle formed ~~on~~ along said upper surface and extending at least partially in a second plane vertically spaced from said first plane; and

solder coating at least a portion of both said upper surface and said obstacle, whereby micro-cracks forming in said solder adjacent to said upper surface will encounter said obstacle.

Claim 18 (previously presented): The solder joint of claim 17, wherein said obstacle comprises a serpentine upper surface.

Claim 19 (previously presented): The solder joint of claim 17, wherein said obstacle comprises an interdigitated strip projecting from said pad.

Claim 20 (previously presented): The solder joint of claim 17, wherein said obstacle comprises a curved edge digit located in a central portion of said pad.

Claim 21 (previously presented): The solder joint of claim 17, wherein said obstacle comprises at least two concentric walls extending outwardly from pad.

Claim 22 (previously presented): The solder joint of claim 17, wherein said obstacle comprises a raised, cross-shaped member extending outwardly from pad.

Claim 23 (previously presented): The solder joint of claim 17, wherein said obstacle comprises a plurality of cylindrical protrusions extending perpendicularly from said pad.

Claim 24 (previously presented): A solder joint for interconnecting an electronic chip to a substrate, comprising:

a first metallic pad having a substantially planar first lower surface for engaging said substrate and a first upper surface including a first plurality of serpentine undulations extending upwardly;

a second metallic pad having a substantially planar second upper surface for engaging said chip and a second lower surface including a second plurality of serpentine undulations extending downwardly; and

solder interconnecting said first upper surface with said second lower surface, whereby micro-cracks forming in said solder adjacent to said first upper surface or said second lower surface will encounter said first plurality of serpentine undulations or said second plurality of serpentine undulations, respectively.